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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/699,537	10/30/2000	Walter L. Moden	2687.3US (94-305.3)	8772

7590 05/08/2002

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EXAMINER
BROCK II, PAUL E

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 05/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/699,537	MODEN, WALTER L.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 26-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 26-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the board that includes a plurality of vias extending therethrough, the solder balls and the providing at least two semiconductor die must be shown or the feature(s) canceled from the claim(s). Further, bond pads extending along a longitudinal axis of the die must be shown or the feature cancelled from the claim. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. In order to avoid abandonment, the drawing informalities noted in Paper No. 9, mailed on December 17, 2001 and repeated above, must now be corrected. Correction can only be effected in the manner set forth in the above noted paper.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 – 4 and 26 – 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eide (USPAT 5313096) in view of Kohno et al. (USPAT 5293068, Kohno).

With regard to claim 1, Eide discloses in figure 10 providing a semiconductor die (20) having a surface having a plurality of bond pads (36) extending along an axis of the die on the surface. Eide discloses in figure 10 providing a substrate (24) having a die side surface, a second attachment surface, at least one via (36) extending through the substrate from the die side surface to the second attachment surface, a plurality of circuits (46), and a plurality of bond pads (56) located on the second attachment surface of the substrate. Eide discloses in figure 10 attaching the surface having a plurality of bond pads thereon of the semiconductor die to the die side surface of the substrate. Eide discloses in figure 10 connecting the plurality of bond pads of the semiconductor die to the plurality of bond pads of the substrate using a plurality of wire bonds (72), the plurality of wire bonds extending through the at least one via extending through the substrate. Eide does not teach that the plurality of bond pads extend along a longitudinal axis. Kohno teaches in figures 3 and 4 a plurality of bond pads (1p) extending along a longitudinal axis of a die (1) on a surface of the die. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the longitudinal layout of bond pads of Kohno in the method of Eide in order to simplify a layout of bond pads.

With regard to claim 2, it is inherent in the method of Eide that an adhesive is applied to a portion of the die side of the substrate to attach the semiconductor die thereto.

With regard to claim 3, Eide discloses in figures 7 and 11 filling (100) at least a portion of the via in the substrate with a sealant (74).

With regard to claim 4, Eide discloses in figures 7 and 11 filling the via in the substrate with a sealant.

Claims 26 – 29 are rejected similar to claims 1 – 4 respectively.

5. Claims 5, 6, 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shen (USPAT 5384689) in view of Kohno et al. (USPAT 5293068, Kohno).

Shen discloses in figures 5 – 7 a method of electrically connecting a semiconductor die (80) to a substrate (60).

With regard to claim 5, Shen discloses in figures 5 – 7 providing a semiconductor die having a plurality of bond pads thereon. Shen discloses in column 3 lines 19 – 24 providing a master board having a plurality of circuit traces thereon. Shen discloses in figures 5 – 7 providing a board having a die side surface, a second attachment surface, at least one via extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of connection points located on the second attachment surface of the board. Shen discloses in figures 5 – 7 providing a plurality of electrical connectors (63) for connecting the plurality of connection points located on the second attachment surface of the board to the circuit traces of the master board. Shen discloses in figures 5 – 7 attaching the semiconductor die to a portion of the die side surface of the board. Shen discloses in figures 5 – 7 connecting the plurality of bond pads of the semiconductor die to the plurality of connection points of the board using a plurality of wire bonds, the plurality of wire bonds extending through the at least one via extending through the board. Shen discloses in column 3, lines 19 – 24 connecting the board and master board using the plurality of electrical connectors on the board to

the plurality of circuit traces on the master board. Shen does not disclose that the connection points are bond pads. Kohno discloses in figure 4 bond pads on a second attachment surface of a substrate (2). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the bond pads of Kohno as the connection points of Shen in order to have a dedicated surface in which to bond a wire to as is well known in the art. Kohno further teaches the plurality of bond pads extend along a longitudinal axis of a die of the surface of the semiconductor die. It would have further been obvious to one of ordinary skill in the art to arrange the bond pads of Shen in the longitudinal direction of Kohno in order to simplify the layout of the bond pads.

With regard to claim 6, Shen discloses in figures 5 – 7 wherein the board includes a plurality of vias extending therethrough.

Claims 30 and 31 are rejected similar to claims 5 and 6 respectively.

6. Claims 8 – 11 and 33 – 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kryzaniwsky (USPAT 5099309) in view of Kohno.

With regard to claim 8, Kryzaniwsky discloses in figures 1a – 1l a method of electrically connecting at least two semiconductor die (5 and 7) to a substrate (40). Kryzaniwsky discloses in figures 1a – 1l providing at least two semiconductor die, each semiconductor die having a surface having a plurality of bond pads extending along an axis of the die on the surface. Kryzaniwsky discloses in figure 9 providing a substrate having a die side surface, a second attachment surface, at least two vias extending through the substrate from the die side surface to the second attachment surface, a plurality of circuits (12), and a plurality of connection points

located on the second attachment surface of the board. Kryzaniwsky discloses in figures 1a – 1l attaching the surface having a plurality of bond pads thereon of a semiconductor die of the at least two semiconductor die to the die side surface of the substrate having the plurality of bond pads of the semiconductor die located over one of the at least two vias extending through the substrate. Kryzaniwsky discloses in figures 1a – 1l connecting (20 and 21) the plurality of bond pads of the semiconductor die to the plurality of connection points of the substrate using a plurality of wire bonds, the plurality of wire bonds extending through the one via extending through the substrate of the at least two vias extending through the substrate. Kryzaniwsky does not disclose that the connection points are bond pads. Kohno discloses in figure 4 bond pads on a second attachment surface of a substrate (2). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the bond pads of Kohno as the connection points of Kryzaniwsky in order to have a dedicated surface in which to bond a wire to as is well known in the art. Kohno further teaches the plurality of bond pads extend along a longitudinal axis of the die of the surface of the semiconductor die. It would have further been obvious to one of ordinary skill in the art to arrange the bond pads of Kryzaniwsky in the longitudinal direction of Kohno in order to simplify the layout of the bond pads.

With regard to claim 9, it is inherent that Kryzaniwsky applies an adhesive to a portion of the die side of the substrate to attach each semiconductor die thereto.

With regard to claim 10, Kryzaniwsky discloses in figures 1a – 1l filling at least a portion of the via in the substrate with a sealant (42).

With regard to claim 11, Kryzaniwsky discloses in figures 7 and 11 filling the via in the substrate with a sealant.

Claims 33 – 36 are rejected similar to claims 8 – 10 respectively.

7. Claims 12, 14 – 16, 37 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kryzaniwsky in view of Kohno and Shen.

With regard to claim 12, similar to the embodiments disclosed by Kryzaniwsky and Kohno as applied to claim 8 above, it is not clear if Kryzaniwsky and Kohno discloses a master board or providing. Shen discloses in figures 5 – 6 and column 3, lines 19 – 24 providing a master board having a plurality of circuit traces thereon and a plurality of electrical connectors for connecting a plurality of bond pads located on a second attachment surface of a board to circuit traces of the master board. It would have been obvious to one of ordinary skill in the art that electrical connectors and master board of Shen in the method of Kryzaniwsky and Kohno in order to create a connection means between a plurality of semiconductor devices and packages.

With regard to claim 14, Kryzaniwsky and Shen does not disclose that the plurality of electrical connectors comprise pins. Pins are well known in the art. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use pins to connect the plurality of semiconductor die to a master board of Kryzaniwsky and Shen in order to make an electrical connection between the die and board as is well known in the art.

With regard to claims 15 and 16, they are rejected similar to claims 10 and 11.

Claims 37 and 39 are rejected similar to claims 12 and 14.

8. Claims 7 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shen and Kohno as applied to claims 5 and 30 above, and further in view of Degani et al. (USPAT 5473512, Degani).

Shen and Kohno do not disclose what comprises the plurality of electrical connectors. Degani discloses in figure 1 a plurality of electrical connectors that comprise solder balls (201 – 204). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the solder balls of Degani in the method of Shen and Kohno in order to electrically connect board wiring layers with master board wiring layers as stated by Degani in column 6, lines 29 – 33.

9. Claims 13 and 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kryzaniwsky, Kohno and Shen as applied to claims 12 and 37 above, and further in view of Degani et al. (USPAT 5473512, Degani).

Kryzaniwsky, Kohno and Shen do not disclose what comprises the plurality of electrical connectors. Degani discloses in figure 1 a plurality of electrical connectors that comprise solder balls (201 – 204). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the solder balls of Degani in the method of Kryzaniwsky, Kohno and Shen in order to electrically connect board wiring layers with master board wiring layers as stated by Degani in column 6, lines 29 – 33.

Response to Arguments

10. Applicant's arguments with respect to claims 1 – 16 and 26 – 39 have been considered but are moot in view of the new ground(s) of rejection.

11. Applicant's arguments filed March 15, 2002 have been fully considered but they are not persuasive.

12. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

13. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

In this case, the suggestion to combine each of the references can be found in the rejection of the respective claims, above, and in the previous office action dated December 17, 2001.

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
May 6, 2002

EDDIE LEE
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